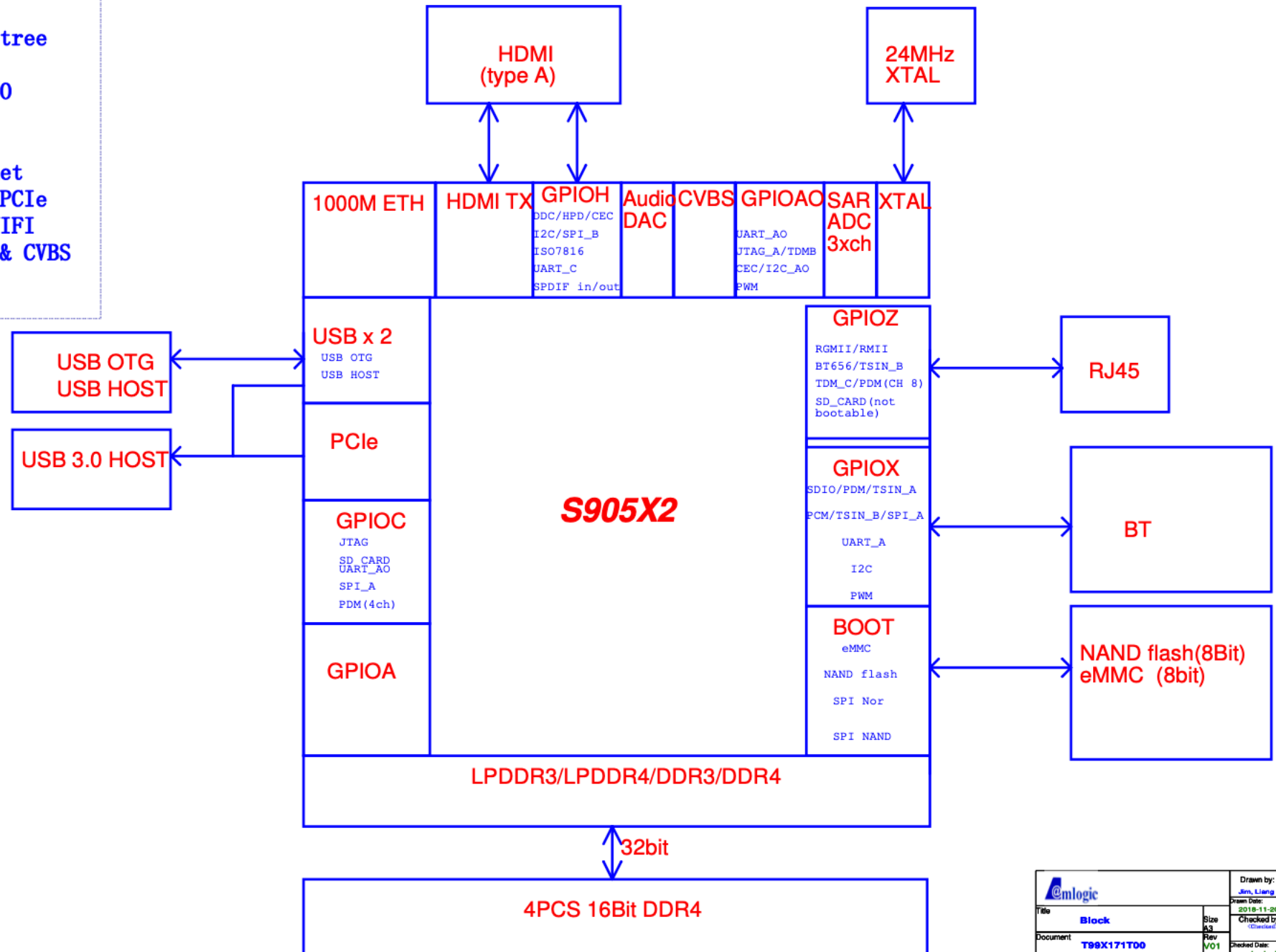


Page Index

- 00- Block
- 00- Power tree
- 01- Power
- 02- CPU I/O
- 03- DDR4
- 04- Flash
- 05- Ethernet
- 06- USB & PCIe
- 07- SDIO WIFI
- 08- Audio & CVBS
- 09- HDMI

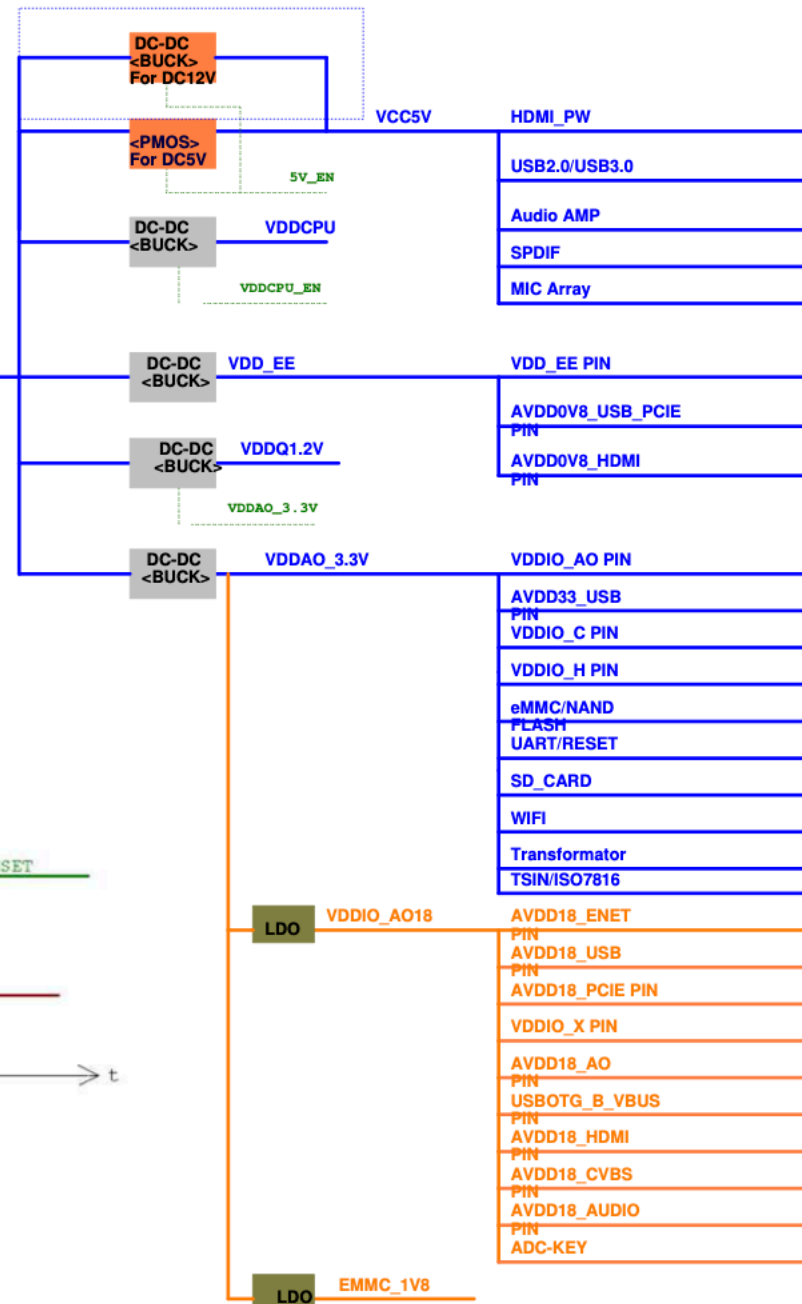
S905X2 REF BOARD DIAGRAM



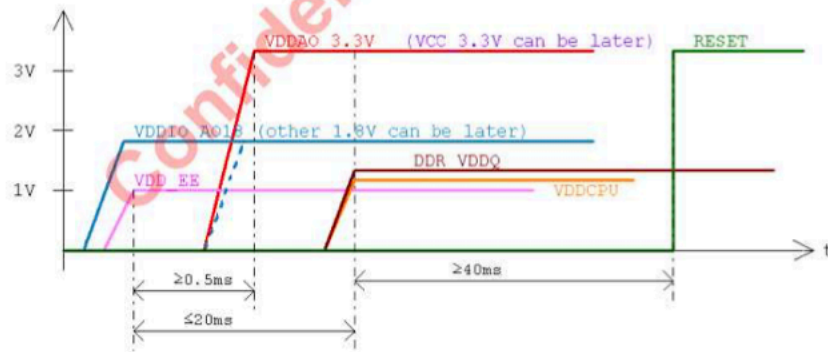
Power Tree

Option:
12V@1A

Default:
5V@2A

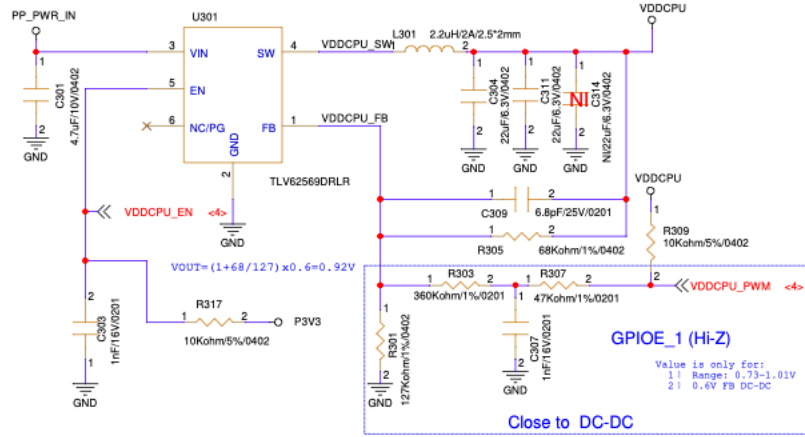


Example power on sequence:



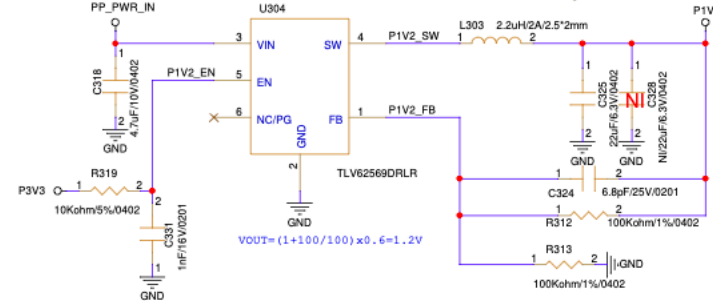
PP_PWR_IN to VDDCPU

Design Max: 2A



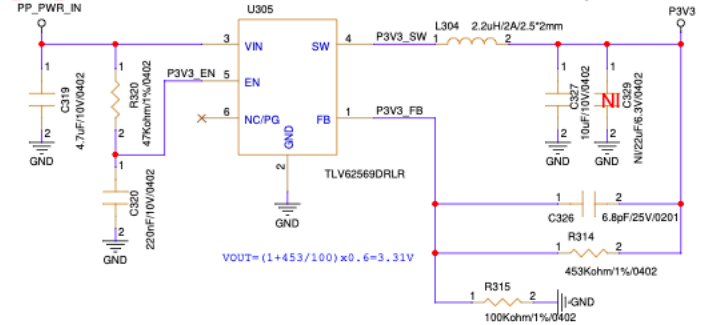
PP_PWR_IN to P1V2

Design Max: 2A



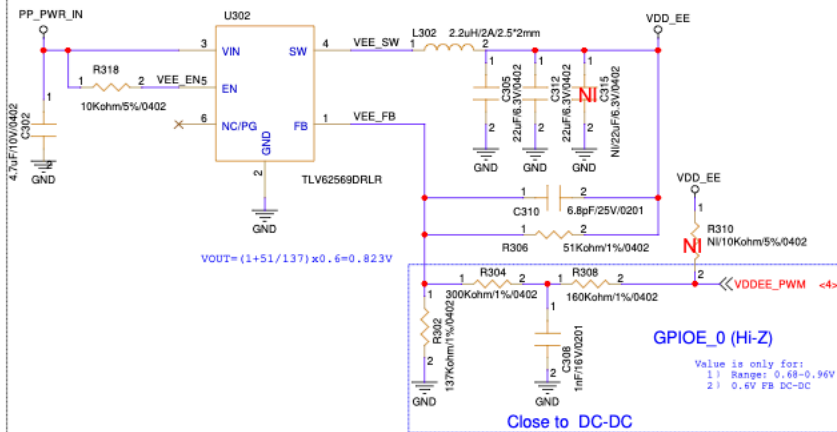
PP_PWR_IN to P3V3

Design Max: 2A



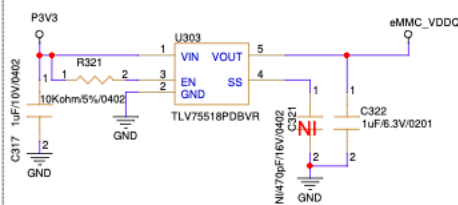
PP_PWR_IN to VDD_EE

Design Max: 2A



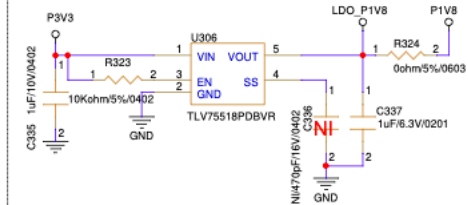
P3V3 to eMMC_VDDQ

Design Max: 500mA



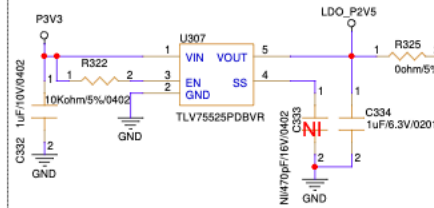
P3V3 to P1V8

Design Max: 500mA



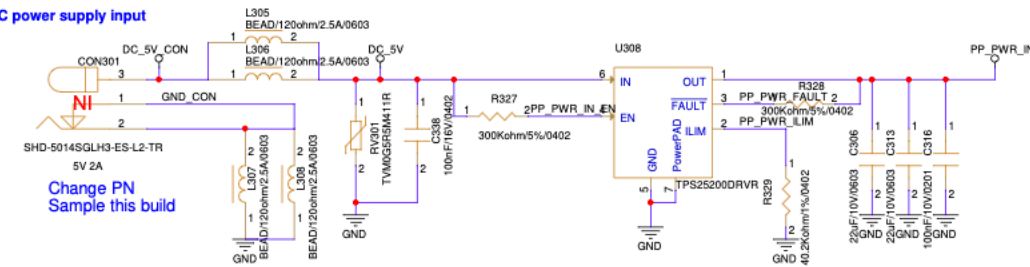
P3V3 to P2V5

Design Max: 500mA



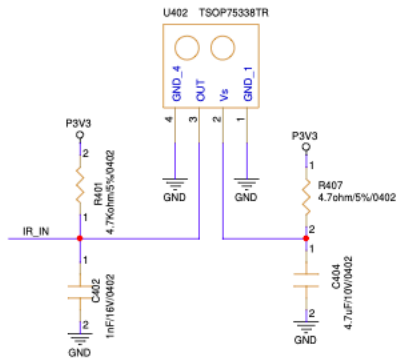
DC power supply input

Change PN
Sample this build

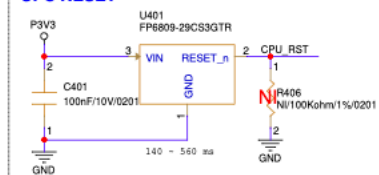


		Drawn by: Jim Liang
Title Power		Drawn Date: 2018-11-20
Document T99X171T00		Checked by:
Date Wednesday, March 27, 2019		Sheet 3 of 15

Remote control receiver

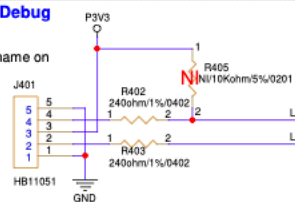


CPU RESET

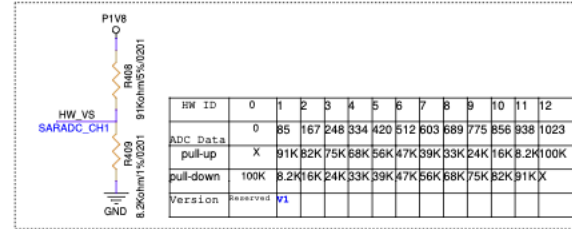
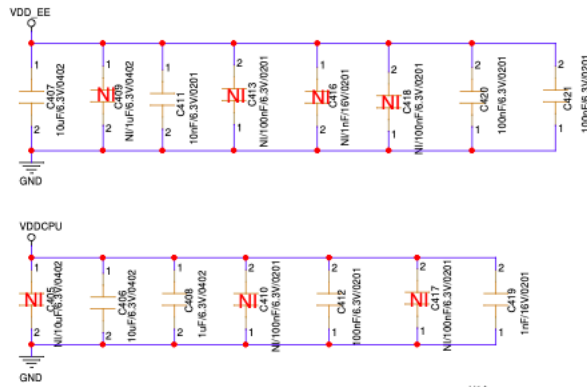
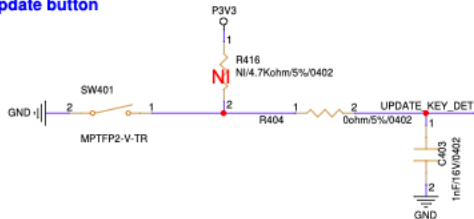


For Linux Debug

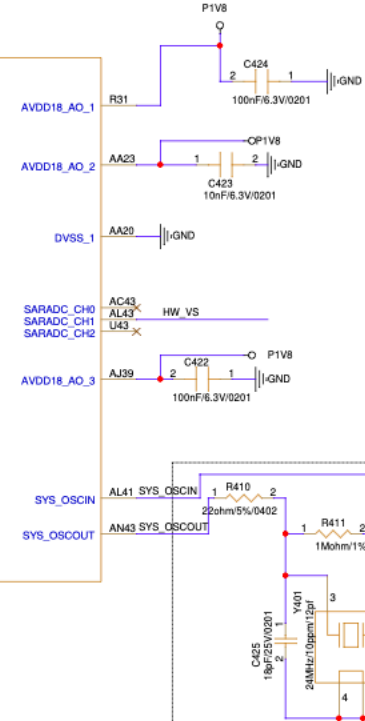
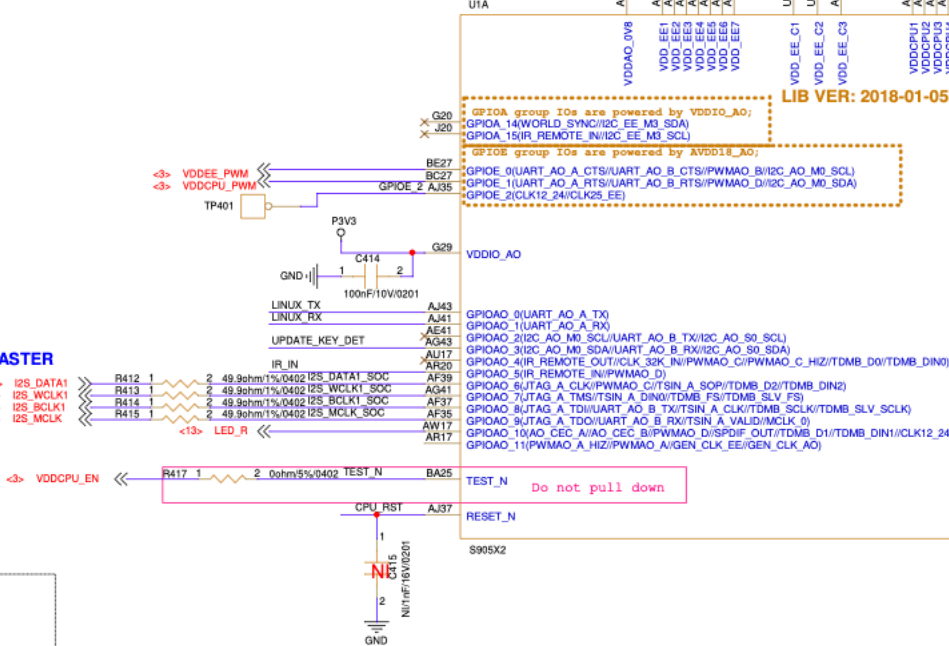
mark signal name on PCB



Update button



HW ID	0	1	2	3	4	5	6	7	8	9	10	11	12
ADC_Data	0	85	167	248	334	420	512	603	689	775	856	938	1023
pull-up	X	91K	82K	75K	68K	56K	47K	39K	33K	24K	16K	8.2K	100K
pull-down	100K	8.2K	16K	24K	33K	39K	47K	56K	68K	75K	82K	91K	X
Version	Reserved	V1											

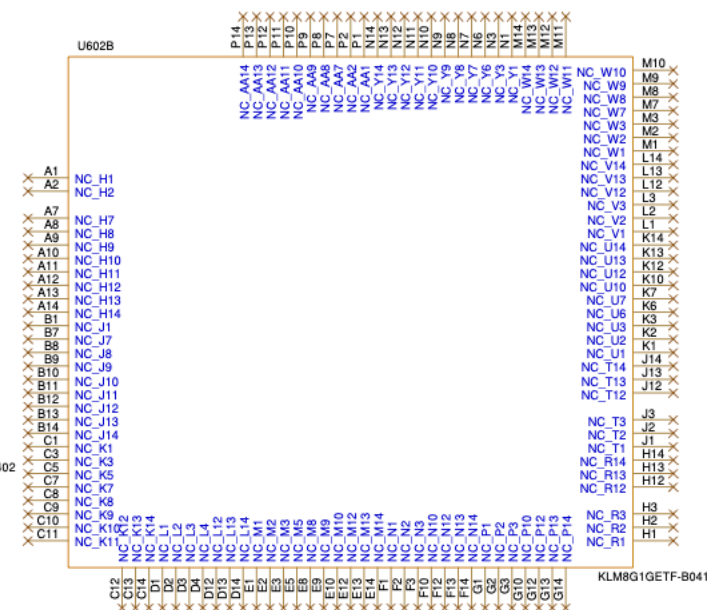


RTC layout notes:
close to CPU, keep XIN/XOUT short,
Do not break GND path

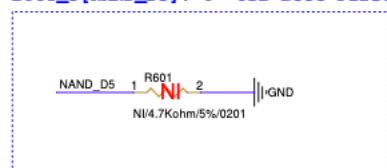
		Drawn by: Jim Liang	
Title: CPU I/O		Drawn Date: 2018-11-20	
Document: T96X171T00		Checked by: checked	
Date: Tuesday, May 07, 2019		Checked Date: checked date	
Sheet: 4		of 16	

Do not route over RFU pins

Note:
Nand flash: 1C4=NC
eMMC: Reserved 4C1=1nF for esd.



BOOT_5[NAND_D5]: 0= USB Boot First



U1G

LIB VER: 2018-01-05

ENET_TXP
ENET_TXNENET_RXP
ENET_RXN

ENET_ATP

ENET_EXTRES

DVSS_3

AVDD18_ENET

VDDIO_Z

GPIOZ_0(ETH_MDIO//ISO7816_CLK/BT656_A_VS//I2C_EE_M0_SDA)
GPIOZ_1(ETH_MDC//ISO7816_DATA/BT656_A_HS//I2C_EE_M0_SCL)GPIOZ_2(ETH_RGMII_RX_CLK//TSIN_B_VALID//TDMC_D0//TDMC_DIN0//PDM_DIN0//SDCARD_D0)
GPIOZ_3(ETH_RX_DV//TSIN_B_SOP//BT656_A_CLK//TDMC_D1//TDMC_DIN1//PDM_DIN1//SDCARD_D1)
GPIOZ_4(ETH_RXD0//TSIN_B_DIN0//BT656_A_DIN0//TDMC_D2//TDMC_DIN2//PDM_DIN2//SDCARD_D2)
GPIOZ_5(ETH_RXD1//TSIN_B_CLK//BT656_A_DIN1//TDMC_D3//TDMC_DIN3//PDM_DIN3//SDCARD_D3)
GPIOZ_6(ETH_RXD2_RGMII//TSIN_B_FAIL//BT656_A_DIN2//TDMC_FS//TDMC_SLV_FS//PDM_DCLK//SDCARD_CLK)
GPIOZ_7(ETH_RXD3_RGMII//TSIN_B_DIN1//BT656_A_DIN3//TDMC_SCLK//TDMC_SLV_SCLK//I2C_EE_M0_SDA//SDCARD_CMD)

CARD port on GPIOZ is not bootable

GPIOZ_8(ETH_RGMII_TX_CLK//TSIN_B_DIN2//BT656_A_DIN4//MCLK_1//I2C_EE_M0_SCL)
GPIOZ_9(ETH_TXEN//TSIN_B_DIN3//BT656_A_DIN5)
GPIOZ_10(ETH_TXD0//TSIN_B_DIN4//BT656_A_DIN6)
GPIOZ_11(ETH_TXD1//TSIN_B_DIN5//BT656_A_DIN7)
GPIOZ_12(ETH_TXD2_RGMII//TSIN_B_DIN6)
GPIOZ_13(ETH_TXD3_RGMII//TSIN_B_DIN7//GEN_CLK_EE)
GPIOZ_14(OD3.3V)(ETH_LINK_LED//I2C_EE_M2_SDA)
GPIOZ_15(OD3.3V)(ETH_ACT_LED//I2C_EE_M2_SCL)

S905X2

C39
A39C41
A41

L26

J26

U29

L33

P1V8

AV39

C701

AR37

AR39

BC43

BE45

AW45

AY41

BA43

BA45

AV41

AU43

AT41

AM37

AM39

AM35

AR45

AR43

R701

R702

R703

R704

R705

R706

R707

R708

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R998

R999

R1000

LIB VER: 2018-01-05

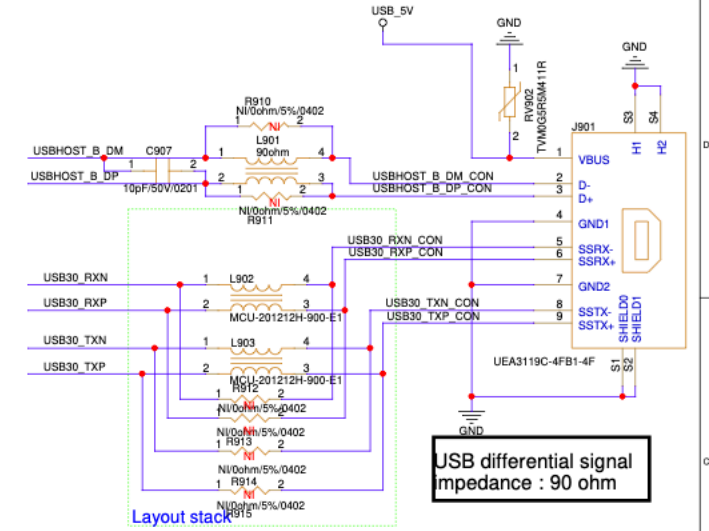
Tolerance 1.8V USBOTG_B_VBUS

For USB OTG application note:
VBUS:1.8V tolerate
USB_VBUS series a 10K_1% to usb jack POWER;
USB_ID series a 200ohm to usb jack ID;

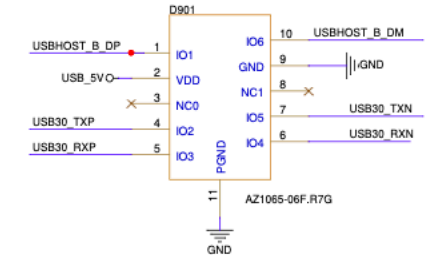
USB differential signal
impedance : 90 ohm

ESD

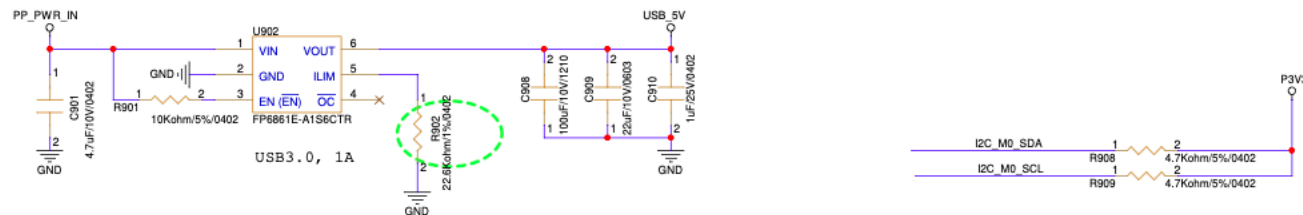
		Drawn by:	Jim, Liang
Title		Drawn Date:	2019-11-20
Document		Checked by:	Checked
T99X171T00		Checked Date:	checked date
Date: Wednesday, March 27, 2019		Sheet	9 of 16

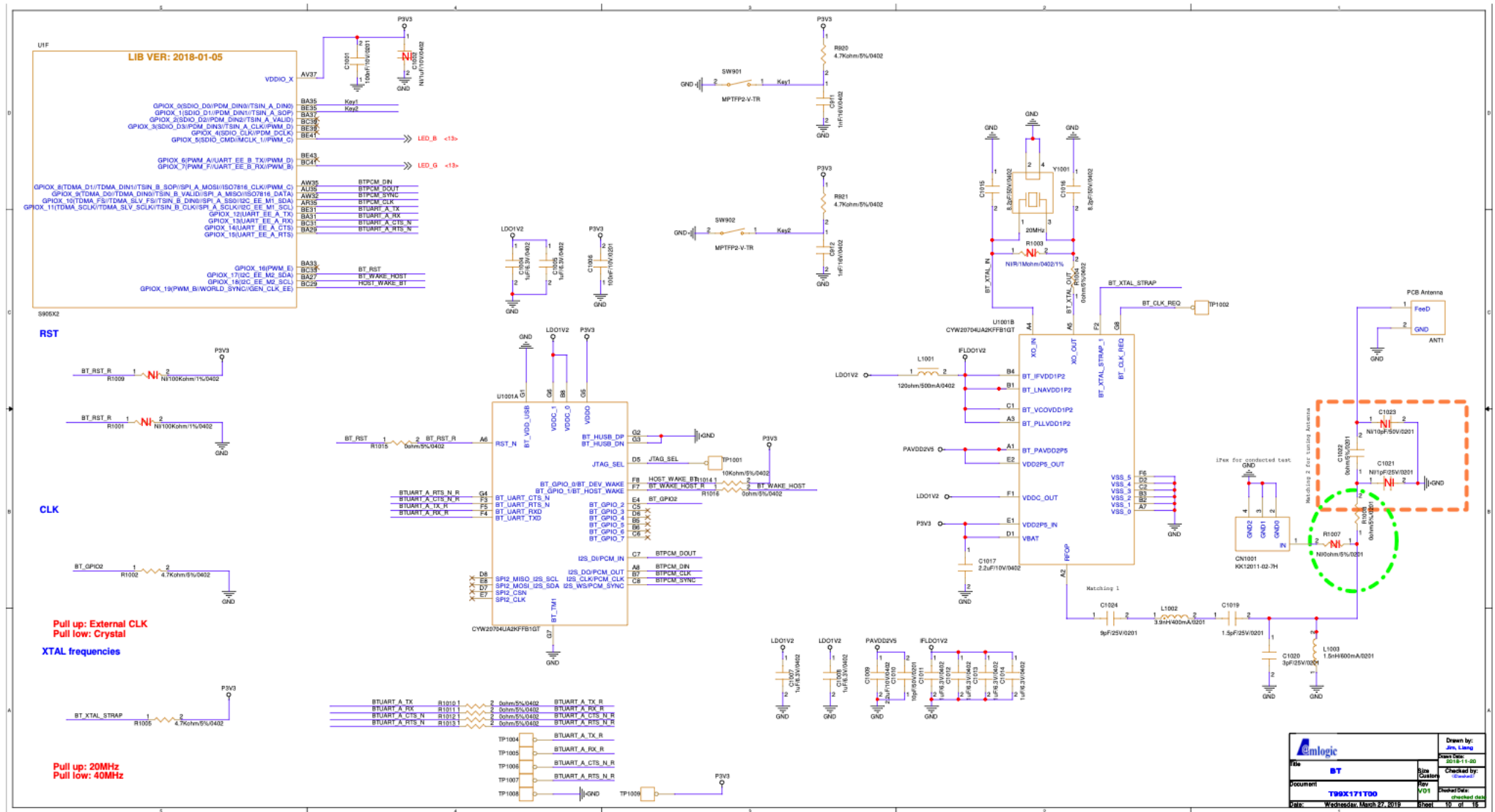


Layout stack



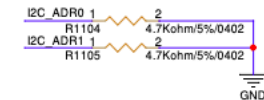
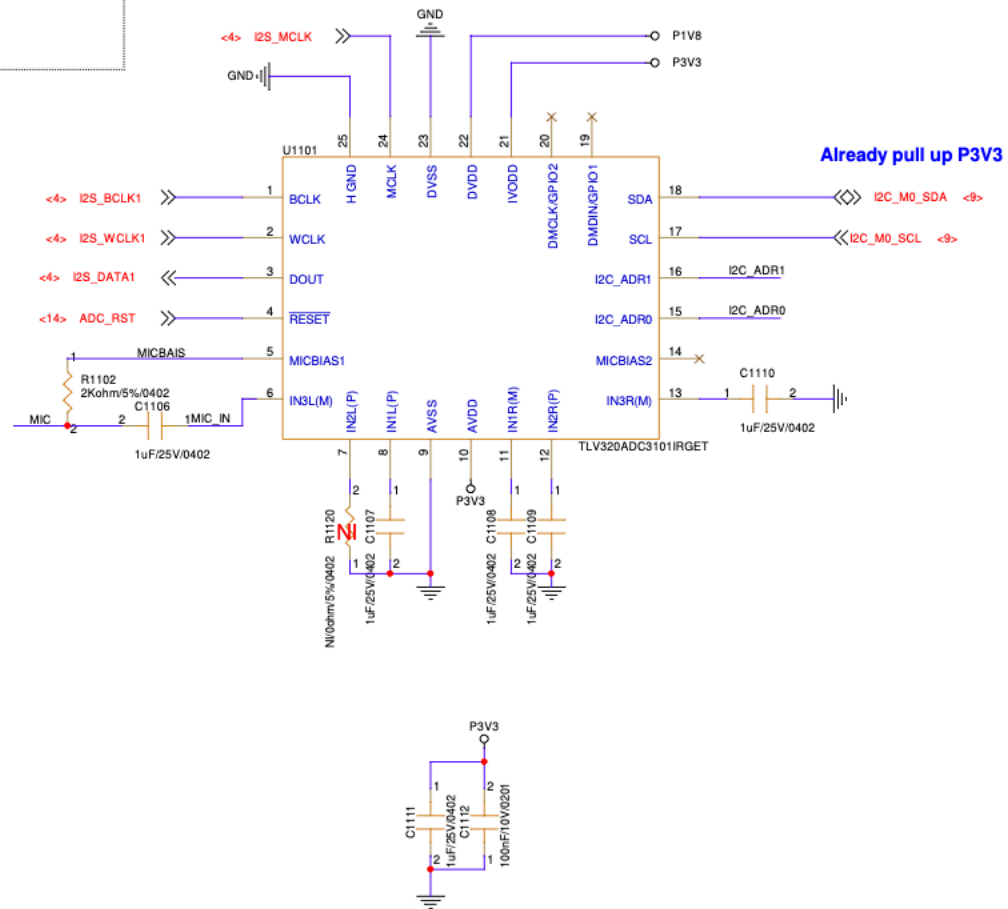
S905X2





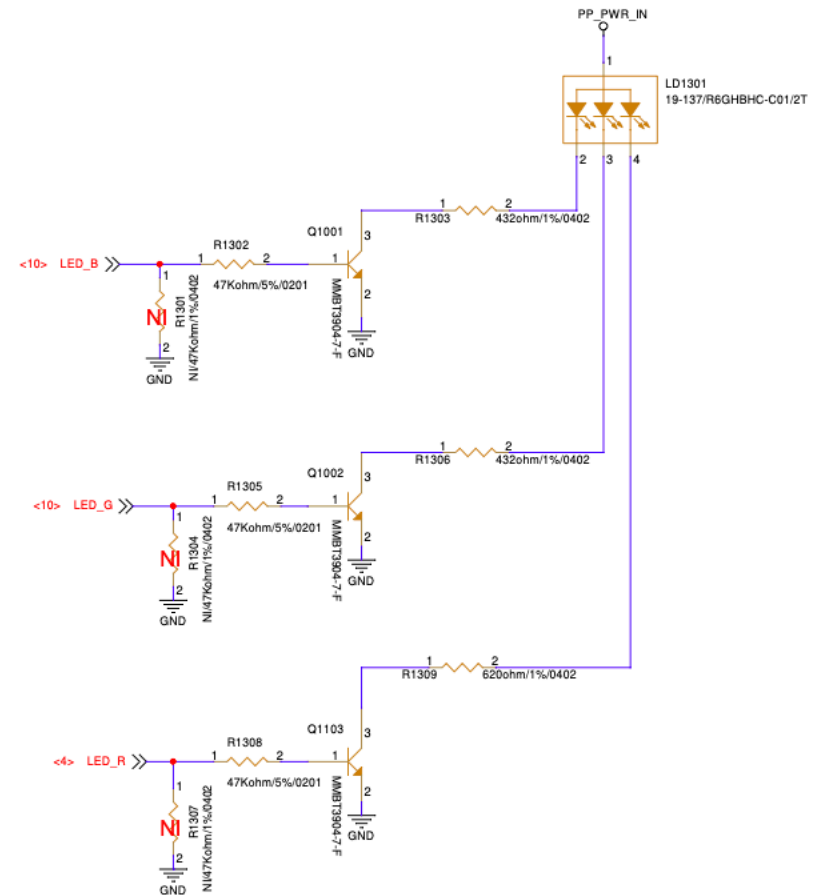
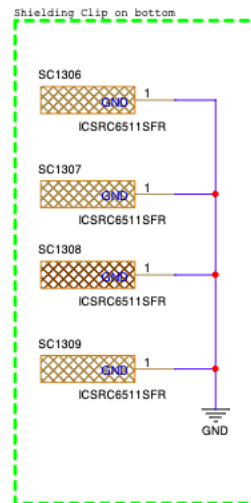
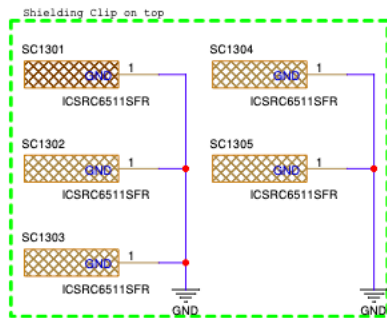
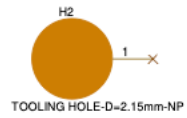
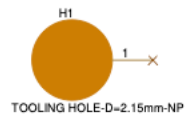
RST>10ns

The diagram shows a circuit for measuring the RST delay. A purple line represents the signal path, starting from the left and labeled 'ADC_RST'. It passes through a yellow zigzag line representing a resistor, labeled 'R1101'. The resistor is connected between points '1' and '2'. Point '2' is connected to a green line representing a signal source, labeled 'NI'10Kohm/5%/0201'. The signal source is connected to ground, represented by a symbol labeled 'GND'.

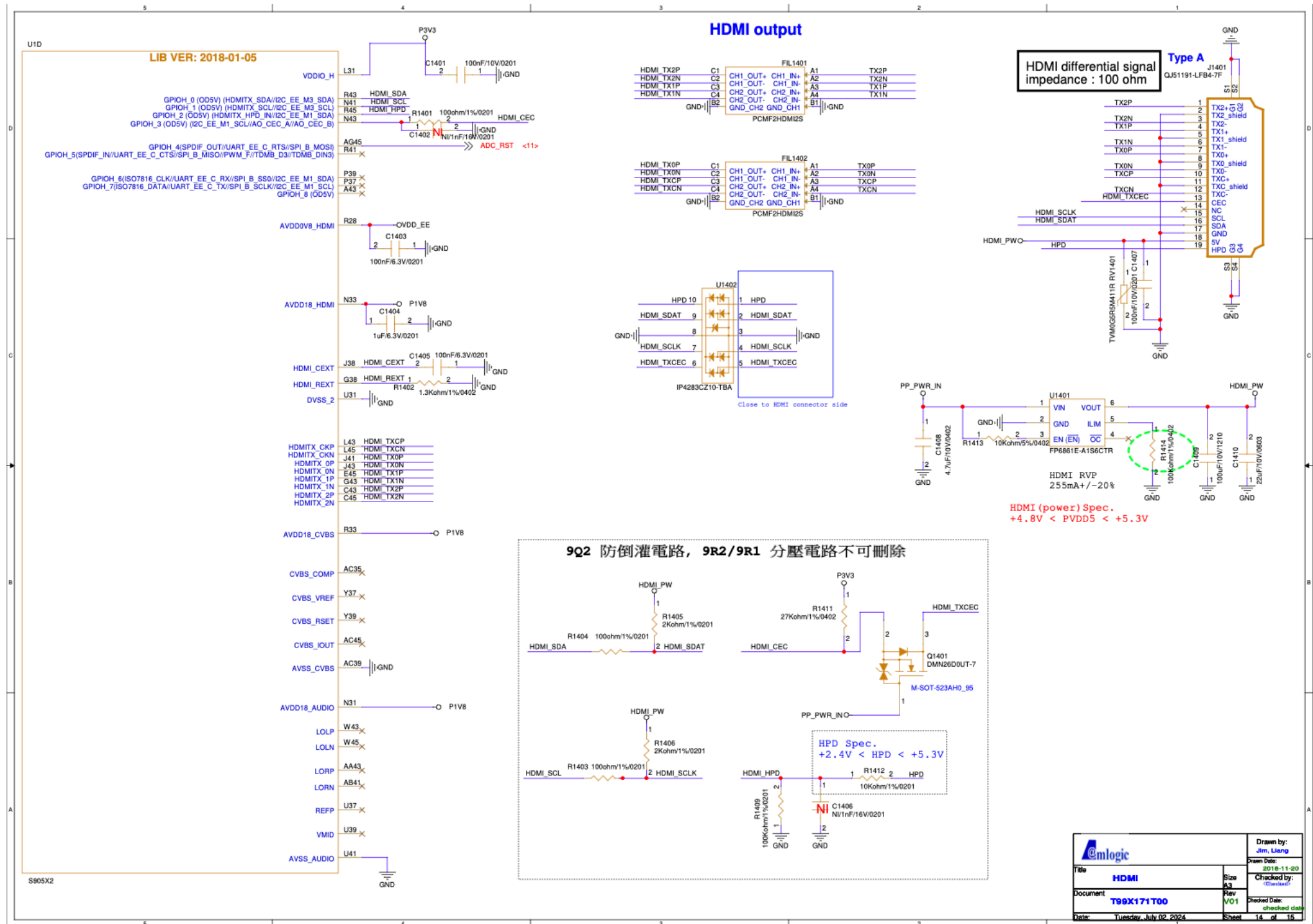


	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

		Drawn by: Jim, Liang	
Title DSP		Drawn Date: 2018-11-20	
Document T99X171T00		Checked by: [checked]	
Date: Wednesday, March 27, 2019		Rev V01	checked date
Sheet		12 of 15	



		Drawn by: Jim, Liang	
Title LED/CLIP		Drawn Date: 2018-11-20	
Document T99X171T00		Size B	Checked by: <checked>
Date: Monday, May 08, 2023		Rev V01	Checked Date: checked date
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Version	Change List	Date
001	First version of T99X171T00	2018/11/01

Version	Change List	Date
002	First version of T99X171T00	2019/03/15

Page 3.

1. OVP and OCP: Change D301 and F301 to TPS25200 solution
2. P1V8 LDO ripple: Change U303 and 306 from 027.01421.005 to JSTLV75518PDBV
3. P2V5 LDO ripple: Change U303 and 306 from 027.01437.005 to JSTLV75525PDBV

Page 4.

4. Slove I2S overshoot and undershoot:Change R412, R413, R414, R415 from 0ohm to 49.9ohm
5. Support wake on BT: Change Net BT_WAKE_HOST fom GPIOX_18 to GPIOAO_2

Page 7.

6. No use for reserve EMI: Delete C702 22p

Page 8.

7. Xtal 25M: Change R802 from 0ohm to 330ohm
8. For phy bringup: add C818 4.7u
9. RGMII TXC/RXC Delay Config: Tx 2ns dealy, pop R814 and R815 nopop
Rx no dealy, pop R813 and R812 nopop

Page 9.

10. USB OTG_ID control pin change to open drain pin: Change OUG_ID from GPIOC_1 to GPIOC_7

Page 10.

11. Xtal 20M: Change C1015 and C1016 from 18p to 8.2p
12. LED (B) change default pull up pin: change LED_B from GPIOAO_11 to GPIO_X5
13. LED (G) change default pull up pin: change LED_G from GPIO_X6 to GPIO_X7

Page 11.

14. ADC change AGND ro GND: Delete R1103, R1106, R1107, R1108, C1113

Page 14.

15. Change HDMI I2C pull up from PP_PWR_IN to HDMI_PW

		Drawn by: Jim, Liang	
Title Revision History		Drawn Date: 2018-11-20	Checked by: <Checked>
Document T99X171T00		Size A3	Rev V01
Date: Wednesday, March 27, 2019		Checked Date: checked date	Sheet 15 of 15